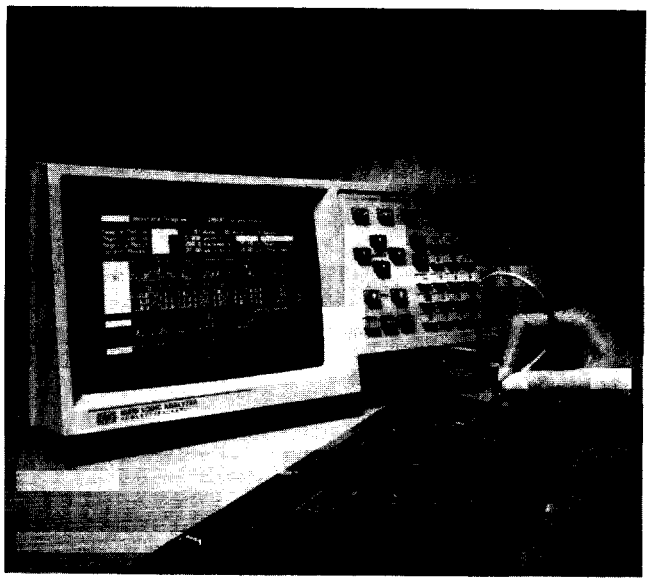
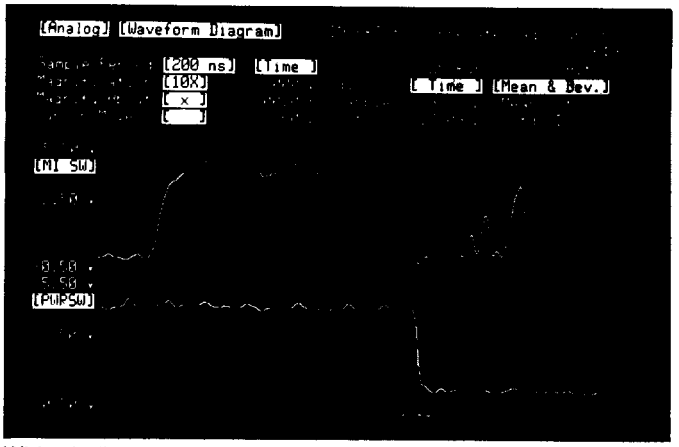
- Built-in two-channel digitizing oscilloscope—50 MHz bandwidth and 200 megasample/second digitizing rate
- Up to 43 state channels and 16 timing channels

NEW

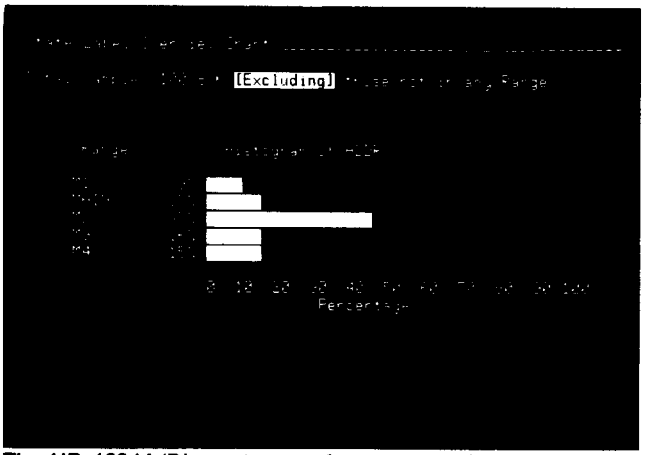


The new HP 1631A/D is a full-featured logic analyzer with a built-in digitizing oscilloscope, enabling the digital hardware designer to make the cross-domain measurements needed to troubleshoot and characterize systems.

- System performance analysis for global view of system activity
- Interactive measurements
- Automatic time-interval measurements



With a built-in oscilloscope, the HP 1631A/D provides two channels of analog analysis plus automatic time-interval measurements.



The HP 1631A/D's system performance analysis mode helps engineers locate problems in program flow, hardware execution, and system activity.

HP 1631A/D Logic Analyzer . . . The One With The Scope

The HP 1631A/D provides a digitizing oscilloscope and a logic analyzer in one low-cost instrument. It offers analog, timing, state, and system performance analysis capabilities function separately or interactively to serve the needs of digital design and test engineers.

The A and D models differ only in state/timing channel width. The HP 1631A provides up to 35 state channels, eight timing channels, and two analog channels. The HP 1631D provides up to 43 state channels, 16 timing channels, and two analog channels.

The One Tool For Every Phase Of Digital Design And Test

A 50 MHz digitizing oscilloscope

- 200 megasample/second digitizing rate for capturing single-shot waveforms
- Two simultaneous channels
- Single-shot time intervals to ±1.5 ns

A complete logic analyzer

- 100 MHz timing analyzer
- Time-interval accuracy to ±1.5 ns
- 25 MHz state analyzer
  - Performance analysis for a global view of the system

Interactive measurements

- Arming and triggering with timing correlation
- Sophisticated triggering features
- Automatic time-interval measurements

Analog Waveform Analysis

Analog waveform analysis provides simultaneous display of up to two channels User-definable labels, wide magnification range, and direct readout of time and voltage between cursors are available.

State Analysis

State listings and waveforms provide displays and windowing of address, data, status, and control line activity. Selectable display modes include binary, octal, decimal, hexadecimal, ASCII, relocation, user-defined mnemonics, and microprocessor-specific mnemonics. You can assign labels, and display and/or trigger on code in terms of relocatable or absolute addresses, or mnemonics.

Timing Analysis

Timing waveform diagrams provide simultaneous display of up to 16 channels, with user-definable labels. Wide magnification range, glitch display, and direct readout of time between cursors are available.

System Performance Analysis

Time interval and event histograms let you view system hardware/software activity or specific modules for performance evaluation. Out-of-spec conditions or bottlenecks in program flow or hardware execution stand out. In addition, the display shows measurement data, including the minimum, maximum, average value, and total measurement time.

LOGIC ANALYZERS

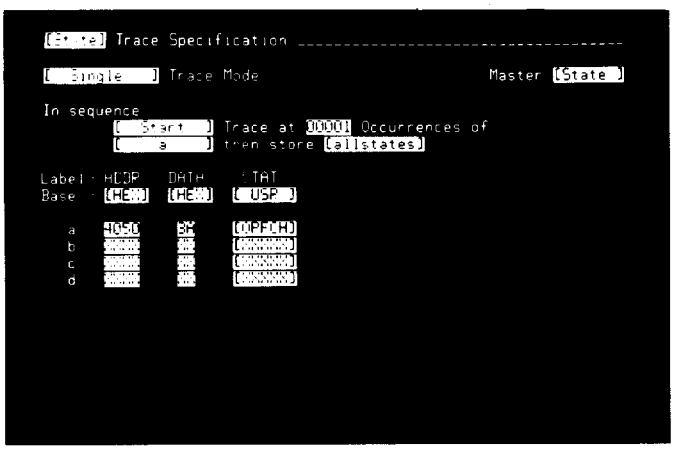
Logic Analyzer With Scope

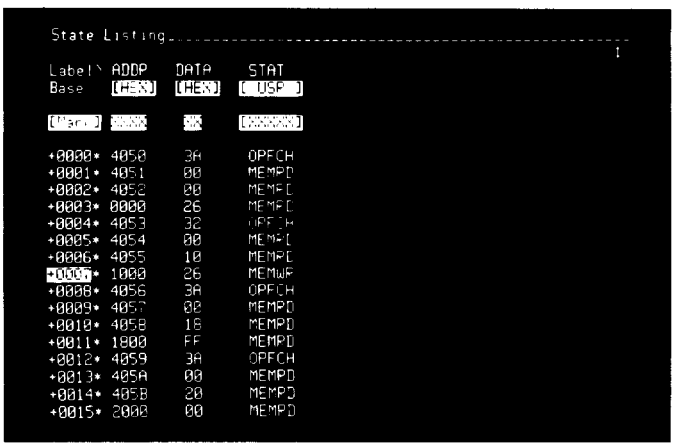
Model 1631A/D

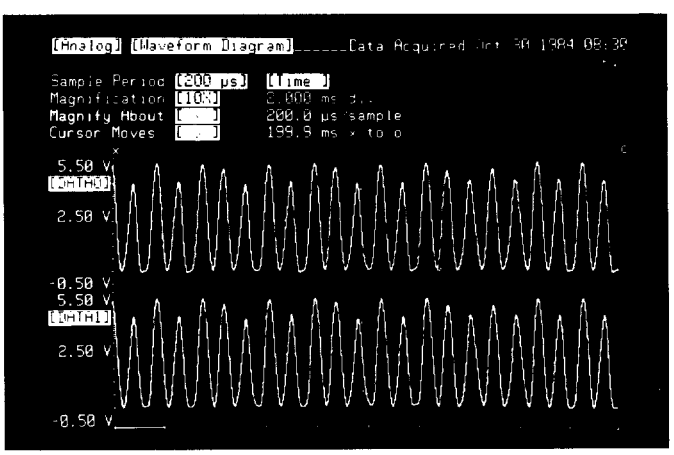
Complete Logic Analysis In A 16-bit Environment

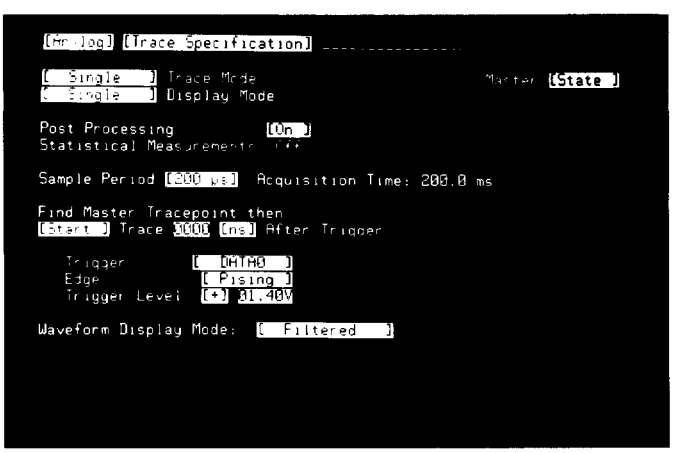
Interactive: State and Analog

Full state analyzer indexing can arm analog waveform acquisition.
Full analog triggering can arm state data acquisition.



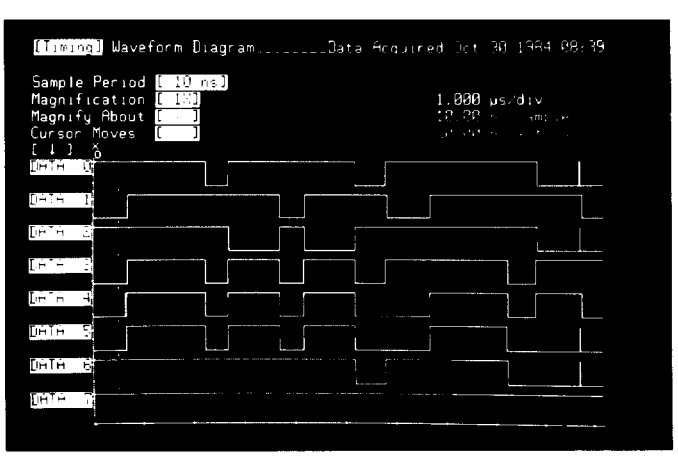


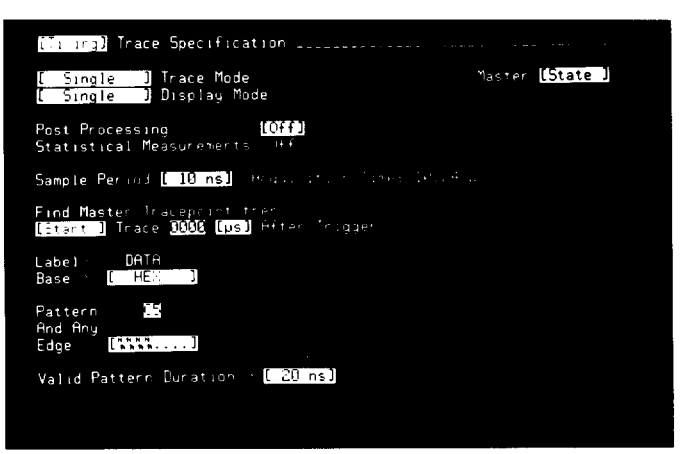




Interactive: State And Timing

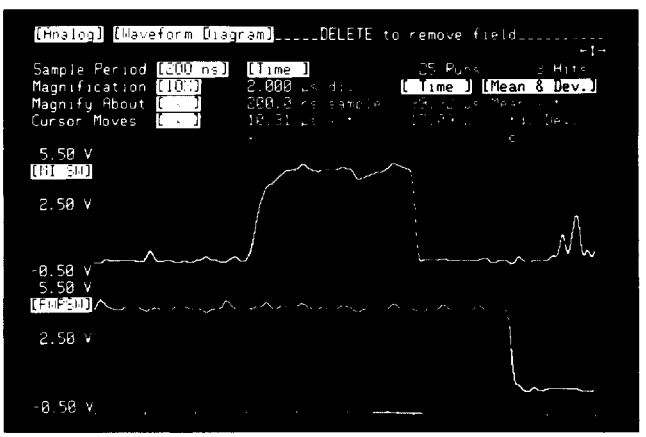
Full state analyzer indexing can arm timing waveform acquisition.
Full timing analyzer indexing can arm state data acquisition.





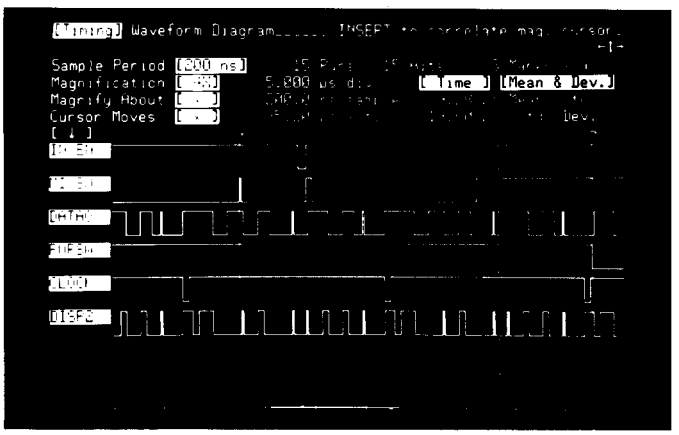
Analog Post-processing

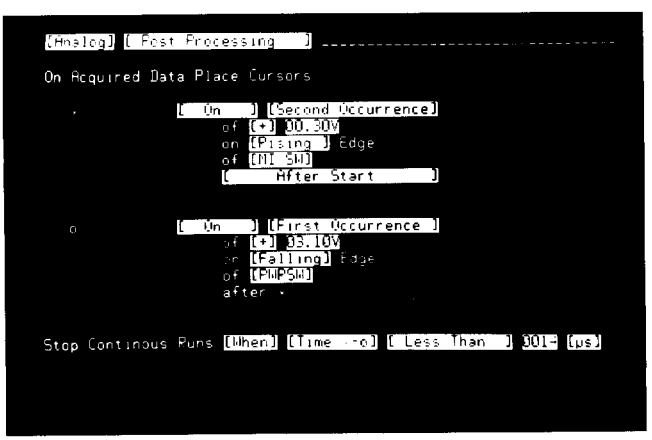
Automatic time-interval measurements are provided through analog X and O cursors, with statistical calculations to enhance accuracy. A search-and-then-stop mode stops waveform acquisition when user-definable trigger conditions are met.

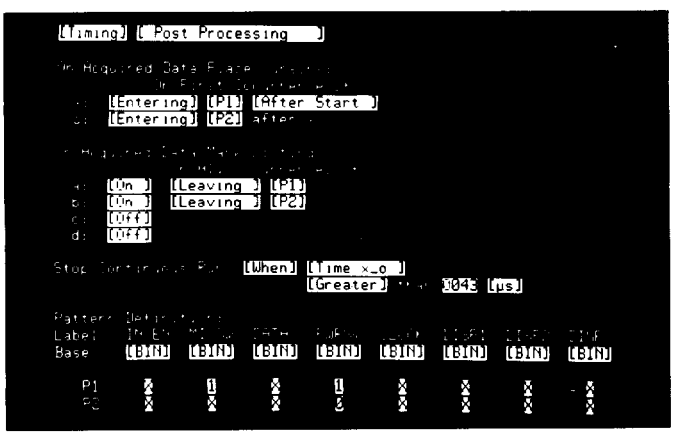


Timing Post-processing

Automatic time-interval measurements are provided through timing X and O cursors, with statistical calculations to enhance accuracy. A search-and-then-stop mode stops timing data acquisitions when user-definable trigger conditions are met.







Inverse Assembly

Displaying program activity in inverse assembly can save many hours in test and debug. No more time-consuming or error-prone conversions from hex because measurement listings appear just as you wrote them, making them easy to compare to source-code listings.

Preprocessor/Interface Modules

HP provides a complete line of microprocessor preprocessors that tailor the HP 1631A/D to specific microprocessors. Preprocessor interface modules contain circuitry that properly formats data, and they provide connection via a microprocessor socket. Software supplied with preprocessors performs inverse assembly for state displays in the selected microprocessor's mnemonics.

A bus preprocessor available for analyzing RS-232C/V.24, RS-449, and HP-IB data bus, and minicomputer interface modules are also available for use with HP logic analyzers.

For more details on these preprocessor/interface modules, please refer to page 416.

HP 1630A/D/G, 1631A/D Specifications

Memory

Data acquisition: 1024 words.
Compare: 16 words, HP 1630A/D, 1631A/D; 16 or 1024 words, HP 1630G.
Memory search: all patterns within a label set may be marked or separately displayed.

State Analysis Mode

Clocks

Clock edges: for each of three ORed clocks, select either or both edges; separate edges of one clock may be selected for multiplexed modes.
Repetition rate, single phase: 25 MHz for single edge of single clock; 20 MHz for any combinations of ORed clocks and edges.
Repetition rate, multiplexed: master clock must follow slave clock by at least 10 ns and precede next slave clock by at least 50 ns.
Pulse width: ≥10 ns at threshold.
Setup time: ≥20 ns.
Hold time: zero.

Data Indexing

Resources: four terms, including the Boolean NOT of each term, ALL patterns or NO pattern; terms may be used as often as needed.
Trigger: up to four resource terms in sequence; final sequence term may use up to four ORed resource terms.
Restart: up to four ORed terms to reinitiate sequence search.
Store qualifiers: up to four ORed resource terms; may be separately defined for each term in the trigger sequence.
Occurrence: to 59 999; applies to final sequence term only.
Compare: width of analyzer by 16 words; trace until "equal to" or "not equal to" with each compare word matched to all 1024 words in memory; compare words may contain "don't care" terms.
Full compare (HP 1630G only): the compare file is the full 1024 states of memory.

Timing Analysis Mode

Clock

Range: 10 ns to 500 ms in 1, 2, 5 sequence.
Accuracy: ± 0.01%.
Glitch: min detectable glitch, 5 ns width at threshold; with glitch detection on, number of timing channels is halved.

Data Indexing

Asynchronous pattern: 20 ns to 1 ms in 1, 2, 5 sequence with accuracy ±20% or 15 ns, whichever is greater; glitch or edge ANDed with asynchronous pattern.
Maximum time delay: approx 2^{18} times the sample period, to 9999 s max.

Cursors: time between dual cursors (x and o) displayed to accuracy of one sample period.
Expansion: X1 to X40 in 1, 2, 4 sequence; standard display shows entire 1k memory at X1.

Analog Analysis Mode (HP 1630G)

Channel 1 And 2 (Vertical)

Probe factors: 1:1, 10:1, or 50:1 probe attenuation factors may be entered to scale the HP 1631A/D to input voltages at the probe tip
Range: 40 mV to 2.5 V full-scale
Bandwidth (−3 dB) dc-coupled: dc to 50 MHz
Dc gain accuracy: ±2.5% of full-scale
Analog-to-digital conversion (ADC) resolution: ±1 LSB, which is ±1.6% of full-scale
Transition time: ≤5.25 ns, 20% to 80% of full-scale

Trigger

Sources: channel 1, channel 2, or external trigger input
Edge: rising or falling edge may be selected for any source

Time Base (Horizontal)

Sample period: 5 ns to 500 ms in a 1-2-5 sequence
Range: 125 ns to 500 s full-scale (10 divisions)
Time base accuracy
Sample period: ±.01%
Time-interval measurement accuracy (equal rise and fall times): single-shot, ±1.5 ns for 5 ns sample period, ±1 sample period for sample periods of 10 ns or greater; continuous, ±.15 times sample period, based on 100 averages
Delay tracepoint: equals trigger plus delay; tracepoint can be delayed from 0 to about 260k sample periods after the trigger

Analog Operating Conditions

Digitizer: two channels are digitized simultaneously
Digitizing technique (real-time digitizing): all data points are digitized at equal selectable increments in time on each acquisition
Digitizing rate: selectable, 2 samples/second to 200 megasamples/second
Voltage resolution: 6 bits, 1 part in 64
Acquisition memory: 1024 samples, 6 bits/channel, 2 channels; up to 1000 samples are used for display; magnifier allows full-screen display from 1000 samples to 25 samples; the entire 1024 sample record can be accessed via HP-IB and HP-IL.

Interactive State/Timing/Analog Analysis Mode

Acquisition: analog, timing, and state data acquisition occur simultaneously
Arming: either of the three analyzers can be master while the remaining two are slave
Master state: the waveform analyzer and the timing analyzer can be simultaneously armed by the full data indexing capability of the state analyzer
Master timing: the waveform analyzer and the state analyzer can be simultaneously armed by the full data indexing capability of the timing analyzer
Master analog (HP 1631A/D): the timing analyzer and the state analyzer can be simultaneously armed by the full analog indexing capability of the waveform analyzer.
Tracepoint alignment: analog, timing, and state acquisition data can be correlated in time
Mixed display: timing channels can be displayed on the same screen with analog channels; the tracepoint and time/div are common to timing and analog in this display mode, and set by the timing analyzer

Software Performance Analysis and Overview Modes

XY Chart: all 1024 events/samples for any label group can be displayed as a chart of order of occurrence by magnitude; max and min vertical limits are user-specified.
Time interval histogram: measures time between start and stop events defined for up to eight time ranges.
Time range: min size, 1 μs.
Display: histogram; min, max, average, and last time reading; total elapsed time; number of samples.
Resolution: for four-bit label group, 250 ns or 0.1% of reading, whichever is greater.
State histogram: sampled occurrence count of events in a label group for up to eight total user-defined ranges or values.
Max count: $2^{63} - 1$.
Resolution: ±0.01%.
Time-positional histogram (HP 1630G only): shows the number of occurrences of an event over time. A time unit is defined, and the analyzer counts the occurrences of a specified event in that time unit. The measurement can be repeated for up to 1023 equal-sized time units.
Typical accuracy of first time unit: −250 ns to +500 ns, +/−0.01% of specified width.
Typical accuracy of subsequent time units: +/−0.01% of specified width.
Linkage histogram (HP 1630G only): shows up to eight module links. A link is defined as a specific state followed immediately by another specific state with no intervening states. Store qualification can be used to acquire states selectively. The measurement can be started on completion of a sequence of up to three resource terms, with restart and occurrence capabilities such as state data indexing.
Max number of definable events: 8.
Max number of definable links: 8.
Max count: $2^{63} - 1$.

LOGIC ANALYZERS
Specifications And Characteristics
Models 1631A/D, 1630A/D/G, 10342B

Measurement Aids
Cursors: two cursors (X and O) are provided for making voltage and time measurements on displayed waveforms. Both absolute and differential values are provided for voltage measurements. Dual cursor time measurements can be made between two points on the same waveform or between two points on different waveforms.

Cursor statistics: X to O cursor statistics are provided for continuous voltage and time measurements: max, min, mean and standard deviation. Single cursor voltage statistics can be obtained between two points on the same waveform or between two points on different waveforms (time only).

Cursor placement: both X and O cursors can be uniquely specified with respect to the tracepoint or acquisition start, by selection of channel 1 or 2, rising or falling edge, voltage level, hold or delay time.

State/Timing/Analog Inputs
State/Timing Probe Inputs
RC: 100k ohm, ±2% shunted by approximately 5 pF at probe body
Minimum swing: 600 mV p-p
Minimum input overdrive (above pod threshold): 250 mV or 30% of input amplitude, whichever is greater
Maximum voltage: ±40 V, peak
Threshold voltage: −9.9 V to +9.9 V in 0.1 V increments
Accuracy: 2.5%, ±120 mV
Dynamic range: ±10 V about threshold
Analog Inputs (HP 1631A/D): channel 1, channel 2, external trigger
Input coupling: dc
Input RC: 1 megohm ±2%, shunted by approximately 14 pF
Maximum safe input voltage: ±40 V (dc + peak ac)

General Characteristics

Labels
Input channel labels: up to eight state, up to 16 timing, user-defined, five-character labels may be assigned bit patterns in any configuration up to 65 (HP 1630G) bits/label. Bits may be used in more than one label and need not be contiguous.

User field: all labels with four bits or less allow mnemonics to be assigned to specific patterns. Primary use is to identify such functions as read, write, opcode, etc.

Relocatable field: up to sixteen module starting locations may be specified, allowing trigger parameters to be based on module names, plus an offset value.

Time-of-day clock: a 24-hour clock prints out the time of data collection on all stored records.
Activity markers: provided in the format display for identifying active inputs.
Non-volatile memory (HP 1630G): the HP 1630G has 8k of EEPROM for internally storing a disassembler. One setup configuration of the instrument can also be stored.

HP-IB Outputs
An HP-IB connector, along with an eight-position switch, is located on the rear panel. Five positions on the switch are used to determine the address, two positions are used to determine "talk-only" for hardcopy and system controller modes.

HP-IL Outputs
An HP-IL connector is located on the rear panel for interfacing.

Programmability
All instrument configurations and acquisition data may be remotely programmed via the HP-IB (IEEE-488) or HP-IL.

Rear-panel BNC Outputs
One BNC output is located on the rear panel with a TTL output. High is ≥2 V into 50 ohms; low is 0.4 V into 50 ohms. The BNC can be programmed from the keyboard to provide the following signals: pulse on state tracepoint, high until state tracepoint, low until state tracepoint, high on last sequence, constant high, constant low, high on timing pattern, probe compensation (HP 1631A/D), and positive edge on analog trigger (HP 1631A/D). A second BNC is located on the rear panel to provide +5 V for the HP 10269B general-purpose probe interface.

Operating Environment
Temperature: 0° to 55° C (+32° to 131° F)
Humidity: up to 95% relative humidity at +40° C
Altitude: to 4600 m (15 000 ft)
Vibration: vibrated in three planes for 15 minutes each with 0.3 mm excursions, 5 to 55 Hz.
Weight: all models ~30 lbs (13.6 kg) net; all models ~40 lbs (18.1 kg) shipping
Power: 115/230 Vac, −22% to +10%; 300 W max; 48–66 Hz
Size: 190 x 426 x 447 mm (7.5 x 16.8 x 17.6 in)

Product Support Package
HP 1630-68705: HP logic analyzer support package
HP 5957-7306: HP logic analyzer service training

Accessories Supplied
One operating manual, one 2.3 m (7.5 ft) power cord, plus the following probes:

HP Model #	10271A	10272A	10273A	10017A
1630A	3	1	—	—
1630D	3	2	—	—
1630G	3	1	3	—
1631A	3	1	—	2
1631D	3	2	—	2

HP 10342B Operating Characteristics

RS-232C (V.24)/449
Asynchronous
Data transfer rates (bits/second): 50, 75, 110, 134.5 150, 300, 600, 1200, 1800, 2000, 2400, 3600, 4800, 7200, 9600 or 19 200
Parity: Odd, even, or none
Bits per character: 6-bit transcode
7-bit ASCII
8-bit ASCII
8-bit EBCDIC
Stop bits per character: 1, 1.5, 2
Synchronous
Data transfer rate: to 72k bits/second
Format: Bit-oriented protocols (BOP)
Synchronous data link control (SDLC)
High-level data link control (HDLC)
X.25 packet mode
Standard network access protocol (SNAP)
Hewlett-Packard data link control (HPDLC)
Burroughs data link control (BDLC)

Advanced data communication control procedure (ADCCP)
Character-oriented protocols (COP)
Binary synchronous communication (BSC)
Digital data communications message protocol (DDCMP)

Selectable: 6, 7, or 8 bits per character
Transmit clock source: data terminal equipment (DTE) or data communications equipment (DCE). Internally selectable on pc-board.

General

Inputs: Three provided: RS-232C (V.24), RS-449, and HP-IB
Outputs: Three mini-probe sockets can be connected to any of the input lines via jumper wires
Signal line loading: RS-232C/449, 1 standard load; HP-IB, 1 LS load (loading at the end of the supplied ribbon cables)
Power requirement: +5 V at 0.65 A

HP 10269B Specifications

Channel width: HP 10269B, 9 probe sockets, 65 data channels, and 3 clock channels.
Qualified clock rate: 25 MHz max.
Input
Impedance: 100 kΩ < 20 pF at interface module connector.
Maximum: ±40 Vdc.
Dynamic range: threshold ±10 V in 0.1 V increments.
Minimum clock pulse width: 10 ns.
Setup and Hold Times
Setup time: 20 ns min.
Hold time: zero.
Power
Power available for interface module: 1.0 A max at +5 Vdc, supplied by HP 1630 Logic Analyzer.
Environmental
Temperature: operating, 0° to +55° C (+32° to +131° F); nonoperating, −40° to +75° C (−40° to +167° F).
Humidity: to 90% at +40° C, noncondensing.
Altitude: operating, 4600 m (15 000 ft); nonoperating, 15 300 m (50 000 ft).

Ordering Information	Price
Logic Analyzers	
HP 1630A (35 channels)	$8600
HP 1630D (43 channels)	$10,630
HP 1630G (65 channels)	$12,100
HP 1631A (35 channels, plus two analog)	$11,000
HP 1631D (43 channels, plus two analog)	$13,000
Support Products	
HP 10269B general-purpose probe interface	$460
HP 10330A HP 1630A/D to HP 1631A/D upgrade kit	$3000
HP 10331A HP 1630A/D to HP 1631A/D upgrade kit, includes ROMs to update for disc-based mass storage	$3500
HP 10340A HP 1630A/D to HP 1630G upgrade kit	$3450
Preprocessors/Interfaces	
Microprocessor Preprocessors - note, inverse assembly is provided on 3½-inch disc	
HP 10300B Z80 interface	$860
HP 10301B Z8001 interface	$960
HP 10302B Z8002 interface	$960
HP 10303B NSC800 interface	$1000
HP 10304B 8085 interface	$860
HP 10305B 8086/8088 interface	$1210
HP 10306B 80186/80188 interface	$2000
HP 10307B 6800/6802 interface	$1100
HP 10308B 6809/6809E interface	$1100
HP 10310B 68005 interface	$1100
HP 10311B 68000/68010 interface	$1300
HP 10312B 80286 interface	$2000
Bus Preprocessors	
HP 10342B bus preprocessor (RS-232C/V.24, RS-449, HP-IB) including inverse assembly	$1200
Minicomputer Interfaces	
HP 10275A PDP-11 UNIBUS interface board	$460
HP 10276A LSI-11 Q-BUS interface board	$510
HP 52126A MULTIBUS interface board	$350
User-definable Interfaces	
HP 10320A user-definable interface module	$250
HP 10321A microprocessor interface kit for the HP 10320A	$225
Connectors	
HP 10322A 40-pin dual in-line package connector for the HP 10320A	$400
HP 10323A 48-pin dual in-line package connector for the HP 10320A	$460
HP 10324A 64-pin dual in-line package connector for the HP 10320A	$560